

# Chapter Finite State Machine Optimization

*Sequential Optimization of Asynchronous and Synchronous Finite-State Machines* Robert M. Fuhrer  
2012-12-06 Asynchronous, or unclocked, digital systems have several potential advantages over their synchronous counterparts. In particular, they address a number of challenging problems faced by the designers of large-scale synchronous digital systems: power consumption, worst-case timing constraints, and engineering and design reuse issues associated with the use of a fixed-rate global clock. Moreover, while for synchronous systems these problems are exacerbated by increasing system size, asynchronous systems promise to scale more gracefully. *Sequential Optimization of Asynchronous and Synchronous Finite-State Machines: Algorithms and*

Tools makes three contributions to the field of sequential optimization for finite-state machines: 1) it introduces several new provably-optimal algorithms for the synthesis and optimization of asynchronous finite-state machines (FSMs); 2) it presents practical software implementations of each of these algorithms; and 3) it introduces a complete new CAD package, called MINIMALIST, binding these tools into a state-of-the-art technology-independent synthesis path for 'burst-mode' asynchronous circuits. Throughout this book, real-world industrial designs are used as benchmark circuits to validate the usefulness of the tools. As an additional benefit, some of the theory and tools also provide new methods for the optimization of synchronous FSMs. **U.S. Government Research**

### **& Development Reports**

1970

**A Synthesis System for Testable and Area-efficient Finite State Machines** Chun-Yeh Liu 1994

*Finite State Machine Datapath Design, Optimization, and Implementation* Justin Davis

2008 Finite State Machine Datapath Design, Optimization, and Implementation explores the design space of combined FSM/Datapath

implementations. The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints, and the use of pipelining for increasing system clock frequency. This is followed by definitions for latency and throughput, with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications. Also, design issues relating to functionality, interfacing, and performance for different types of memories commonly found

in ASICs and FPGAs such as FIFOs, single-ports, and dual-ports are examined. Selected design examples are presented in implementation-neutral Verilog code and block diagrams, with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms. A working knowledge of Verilog, logic synthesis, and basic digital design techniques is required. This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL.

**Sequential Circuit Synthesis at the Gate Level** Ellen Marie Sentovich 1993

**Formal Methods in VLSI System Design** Adnan Aziz 1996

**SystemVerilog for Hardware Description** Vaibbhav Taraate 2020-06-10 This book introduces the reader to FPGA based design for RTL synthesis. It describes simple to complex RTL design scenarios using SystemVerilog. The book builds the story from basic

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fundamentals of FPGA based designs to advance RTL design and verification concepts using SystemVerilog. It provides practical information on the issues in the RTL design and verification and how to overcome these. It focuses on writing efficient RTL codes using SystemVerilog, covers design for the Xilinx FPGAs and also includes implementable code examples. The contents of this book cover improvement of design performance, assertion based verification, verification planning, and architecture and system testing using FPGAs. The book can be used for classroom teaching or as a supplement in lab work for undergraduate and graduate coursework as well as for professional development and training programs. It will also be of interest to researchers and professionals interested in the RTL design for FPGA and ASIC.

A Binary Decision Diagram Approach for Finite State Machine Encoding Pi-Fuang Chen 1997

*Designing Effective Evolutionary Computations* Kumar Hemachandra Chellapilla 2005  
The Harmonic Mind: Cognitive architecture Paul Smolensky 2006 An integrated connectionist/symbolic architecture of the mind/brain, applied to neural/genomic realisation of grammar; acquisition, processing, and typology in phonology and syntax; and foundations of cognitive explanation. Despite their apparently divergent accounts of higher cognition, cognitive theories based on neural computation and those employing symbolic computation can in fact strengthen one another. To substantiate this controversial claim, this landmark work develops in depth a cognitive architecture based in neural computation but supporting formally explicit higher-level symbolic descriptions, including new grammar [Illegible]. Detailed studies in both phonology and syntax provide arguments that these grammatical theories and their

neural network realisations enable deeper explanations of early acquisition, processing difficulty, cross-linguistic typology, and the possibility of genomically [Illegible] universal principles of grammar. Foundational questions concerning the explanatory status of symbols for central problems such as the unbounded productivity of higher cognition are also given proper treatment. science through tutorial chapters and numerous expository boxes providing background material from several disciplines. Examples common to different chapters facilitate the transition from more basic to more sophisticated treatments. Details of method, formalism, and foundation are presented in later chapters, offering a wealth of new results to specialists in psycholinguistics, language acquisition, theoretical linguistics, computational linguistics, computational neuroscience, connectionist modelling, and philosophy of mind.

*Application-tuned Processor*

*Architectures* Timothy Sherwood 2003

**Synthesis of Finite State Machines** Timothy Kam

2013-03-09 Synthesis of Finite State Machines: Functional Optimization is one of two monographs devoted to the synthesis of Finite State Machines (FSMs). This volume addresses functional optimization, whereas the second addresses logic optimization. By functional optimization here we mean the body of techniques that: compute all permissible sequential functions for a given topology of interconnected FSMs, and select a 'best' sequential function out of the permissible ones. The result is a symbolic description of the FSM representing the chosen sequential function. By logic optimization here we mean the steps that convert a symbolic description of an FSM into a hardware implementation, with the goal to optimize objectives like area, testability, performance and so on. Synthesis of Finite State Machines: Functional

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Optimization is divided into three parts. The first part presents some preliminary definitions, theories and techniques related to the exploration of behaviors of FSMs. The second part presents an implicit algorithm for exact state minimization of incompletely specified finite state machines (ISFSMs), and an exhaustive presentation of explicit and implicit algorithms for the binate covering problem. The third part addresses the computation of permissible behaviors at a node of a network of FSMs and the related minimization problems of non-deterministic finite state machines (NDFSMs). Key themes running through the book are the exploration of behaviors contained in a non-deterministic FSM (NDFSM), and the representation of combinatorial problems arising in FSM synthesis by means of Binary Decision Diagrams (BDDs). Synthesis of Finite State Machines: Functional Optimization will be of interest to researchers and designers in logic synthesis, CAD and

design automation.

*Hardware for Soft Computing and Soft Computing for Hardware* Nadia Nedjah  
2013-11-18 Single and Multi-Objective Evolutionary Computation (MOEA), Genetic Algorithms (GAs), Artificial Neural Networks (ANNs), Fuzzy Controllers (FCs), Particle Swarm Optimization (PSO) and Ant colony Optimization (ACO) are becoming omnipresent in almost every intelligent system design. Unfortunately, the application of the majority of these techniques is complex and so requires a huge computational effort to yield useful and practical results. Therefore, dedicated hardware for evolutionary, neural and fuzzy computation is a key issue for designers. With the spread of reconfigurable hardware such as FPGAs, digital as well as analog hardware implementations of such computation become cost-effective. The idea behind this book is to offer a variety of hardware designs for soft computing techniques that can

be embedded in any final product. Also, to introduce the successful application of soft computing technique to solve many hard problems encountered during the design of embedded hardware designs. Reconfigurable embedded designs for GAs, ANNs, FCs and PSO are presented and evaluated. Also, the application of quantum-based evolutionary computation and multi-objective evolutionary computation as well as ACO are applied to solve hard problems related to circuit synthesis, IP assignment, mapping and routing of applications on Network-On-Chip infrastructures.

### Computational Intelligence

Andries P. Engelbrecht 2002  
"Computational Intelligence: An Introduction offers an in-depth exploration into the adaptive mechanisms that enable intelligent behaviour in complex and changing environments. The main focus of this text is centred on the computational modelling of biological and natural

intelligent systems, encompassing swarm intelligence, fuzzy systems, artificial neural networks, artificial immune systems and evolutionary computation."  
"Computational Intelligence: An Introduction is essential reading for third and fourth year undergraduate and postgraduate students studying CI. The first edition has been prescribed by a number of overseas universities and is thus a valuable teaching tool. In addition, it will also be a useful resource for researchers in Computational Intelligence and Artificial Intelligence, as well as engineers, statisticians, operational researchers, and bioinformaticians with an interest in applying AI or CI to solve problems in their domains."--BOOK JACKET.

### **State Minimization of Finite State Machines Using Implicit Techniques**

Timothy Yee-kwong Kam 1995  
*Finite State Machine Verification, Test, and Minimization* Sezer Gören 2003

### **Logic Synthesis for FSM-Based Control Units**

Alexander Barkalov 2009-11-25  
This book presents the hardware implementation of control algorithms represented by graph-schemes of algorithm. It includes new methods of logic synthesis and optimization for logic circuits of Mealy and Moore FSMs oriented on both ASIC and FPLD.

### **Logic Synthesis for Finite State Machines Based on Linear Chains of States**

Alexander Barkalov 2017-06-24  
This book discusses Moore finite state machines (FSMs) implemented with field programmable gate arrays (FPGAs) including look-up table (LUT) elements and embedded memory blocks (EMBs). To minimize the number of LUTs in FSM logic circuits, the authors propose replacing a state register with a state counter. They also put forward an approach allowing linear chains of states to be created, which simplifies the system of input memory functions and, therefore, decreases the number of LUTs in the resulting FSM circuit. The

authors combine this approach with using EMBs to implement the system of output functions (microoperations). This allows a significant decrease in the number of LUTs, as well as eliminating a lot of interconnections in the FSM logic circuit. As a rule, it also reduces the area occupied by the circuit and diminishes the resulting power dissipation. This book is an interesting and valuable resource for students and postgraduates in the area of computer science, as well as for designers of digital systems that included complex control units

### **Finite State Machine Logic Synthesis for Complex Programmable Logic**

**Devices** Robert Czerwinski  
2013-01-12 This book is a monograph devoted to logic synthesis and optimization for CPLDs. CPLDs' macrocell can also be interpreted as programmable AND-fixed OR structure, well known as PAL-based structure. The question is: what should be done when the number of implicants representing function exceeds

the number of product terms available in a logic block. The answer is ... in the book. Logic synthesis and optimization methods dedicated for PAL-based structures are proposed. The methods strive to find the optimum fit for the combinational logic and finite state machines to the structure of the logic device and aim at area and speed optimization. The theoretical background and complete strategies are richly illustrated with examples and figures.

**Logic Optimization of Interacting Components in Synchronous Digital Systems** Yosinori Watanabe  
1994

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